EE 4305 - Computer Architecture

EE Elective, CpE Minor Required Course - Spring 2021

2020-2021 Catalog Course Description:
Advanced assembly language programming techniques. Memory design principles. Virtual memory. Cache memory. Processor design. Pipelined and Reduced Instruction Set Computers (RISC). Advanced microprocessor features. (3hrs lecture, 3hrs lab)

Prerequisites:
EE2325 - Microcomputer System Design

Educational Goals:

Building on the basics learned from EE1315 and EE2325, students will learn advanced digital design techniques. In particular, we focus on register transfer level (RTL) designs utilizing FPGA and Hardware Description Language (HDL) CAD tools.

Today's microprocessors are designed and verified using CAD tools and programmable devices such as FPGA. This course will expose students to VHDL/Verilog and FPGA which will serve as the basic tools for register-transfer level design. The design steps of a processor include instruction set design, physical data path design, and the corresponding control circuit design. The lecture covers all of these topics and related principles. In addition, details of processor design steps are learned through hands-on FPGA labs. In the lab, students will use an FPGA educational board to first implement simple combinational and sequential circuits and then a working processor in the last few labs. MIPS-32 architecture is used for both in the lab and lectures.

Advanced processor design techniques such as pipelining, branch prediction, multiple issues, etc. will be learned. In addition, students will learn single and multi-level caches, virtual memory, and multi-core/processor design basics.

Course Outcomes (Students should …):

- Learn basic components of FPGA (7)
- Learn the basic language of VHDL (7)
- Apply VHDL in FPGA implementation and learn test steps through hands-on labs (7)
- Learn to write and test finite state machines in VHDL on FPGA implementation (1,7)
- Learn to use FPGA as a hardware tool for designing complex digital systems (1,7)
- Learn to design an instruction set of a basic processor (1,7)
- Learn the data path of microprocessors instructions (1)
- Understand the function of buses connecting the microprocessor with memory and I/O devices, and the steps required to read or write a memory or I/O devices (1,7)
- Learn to design cache memory systems (1)
- Learn to use VHDL for design of a RISC processor (1,7)
- Introduce the basic principle of pipelining in modern microprocessor design (1)
- Learn modern multiprocessor architectures (1,2)

Relationship to EE Program Objectives:

- Introduces advanced digital systems and computer architectures.
- Applies fundamentals of digital logic design and microprocessors to the design of processors and memory subsystem.
- Exposes students to HDL.
- Experience implementation of a simple processor and digital systems using FPGA.
- Introduce data path and pipelining

EE 4305: Syllabus – Spring 2021 (Draft)

Professor: Dr. Taek Kwon, Office: 253 MWAH, Email*: tkwon@d.umn.edu*
Office Hours: Ad Hoc Zoom meetings, web: www.d.umn.edu/~tkwon
Lecture: Remote online-set class times, Lecture by Zoom meetings at 1:00-1:50PM on MWF
Lab: MWAH 41 (only if a student does not have a PC), Zoom check-off: 1-4pm Th,
Textbook: David Patterson and John Hennessy, *Computer Organization and Design: The Hardware/Software Interface, 5*th Ed., Morgan Kaufmann (Elsevier Inc), 2014.
Computer Usage: VHDL, Xilinx Vivado 2019, MIPS assembler simulator, Nexys-4 DDR (Nexys A7) FPGA Trainer Board
Assessment: Lab: 35%, Attendance: 3%, Midterm: 27%, Final: 35%

Dates	Topics	
1/13,15	Programmable logic devices, Gate array ASIC	Lec note
1/20,22	FPGA architecture, RTL and VHDL design intro, IEEE 1164	Lec note, lab#1
1/25,27,29	VHDL entity, architecture, concurrent statements, and process	Lec note, lab#2
2/1,3,5	VHDL Port map, libraries, packages, attributes and events in process	Lec note, lab#3
2/8,10,12	VHDL state machine implementation, do and don'ts	Lec note, lab#4
2/15,17,19	MIPS instruction set	Chap 2, lab #5
2/22,24,26	MIPS instruction set	Chap 2, lab #6
3/1,3,5	Single Cycle MIPS processor design	Chap 4
3/3	Midterm Exam (during the same lecture hour, on-line)	
3/10,12	Single-Cycle MIPS processor design	Chap 4
3/15,17,19	Multi-Cycle MIPS processor design	Lec note, lab #7
3/22,24,26	Multi-Cycle MIPS processor design, Pipeline concept	Chap 4, lab #8
3/29,31,4/2	Pipelined processor designs	Chap 4, lab #9
4/5,7,9	Pipelined processor designs	Chap 4, lab #10
4/12,14,16	Cache memory design	Chap 5, lab #11
4/19,21,23	Multiprocessors	Lec note,
4/26	Last day of class, review	
5/3	Final Exam, Monday, 12:00-1:50pm	

Student outcomes addressed by this course:
(1) an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics
(2) an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors
(7) an ability to acquire and apply new knowledge as needed, using appropriate learning strategies.

Students with disabilities: It is the policy and practice of the University of Minnesota Duluth to create inclusive learning environments for all students, including students with disabilities. If there are aspects of this course that result in barriers to your inclusion or your ability to meet course requirements such as time limited exams, inaccessible web content, or the use of non-captioned videos, please notify the instructor as soon as possible. You are also encouraged to contact the Office of Disability Resources to discuss and arrange reasonable accommodations. Call 218-726-6130 or visit the Disability Resources web site for more information.

Academic Integrity: Academic dishonesty tarnishes UMD's reputation and discredits the accomplishments of students. Academic dishonesty is regarded as a serious offense by all members of the academic community. UMD's Student Academic Integrity Policy.

Makeup exams: not available, not provided.